Product Specification Datasheet

TNQS854XM-CD150

40G QSFP+ SR4 Optical Transceiver

The 40G QSFP+ SR4 is a Four-Channel, Pluggable, Parallel, QSFP+ Transceiver for 40 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 40 Gbps bandwidth.one version is each lane can operate at 10.5Gbps up to 100m using OM3 or 150m using OM4 Multimode fiber, another version is each lane can operate at 10.5Gbps up to 300m using OM3 or 400m using OM4 Multimode fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses a 12 fiber MTP (MPO) connector. This module incorporates proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Features

- Supports 1.06 to 10.5Gb/s bit rates per Channel
- Four-Channel, 1x12 MPO receptacle
- Hot pluggable QSFP+ form factor
- VCSEL 850nm array Technology
- 100m on OM3 MMF, 150m on OM4 MMF
- Built-in digital diagnostic functions
- Low power consumption < 1.5W
- Unretimed XLPPI electrical interface
- Operating case temperature: 0~70℃

Applications

- 40GBASE-SR4 40G Ethernet
- Datacom/Telecom switch & router connections
- Data Aggregation and Backplane Applications
- Proprietary Protocol and Density Applications
- Other optical links

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	Ts	-20	85	℃	
Relative Humidity	RH	0	85	%	
Damage Threshold, per Lane	DT	3.4		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

General Operating Characteristics

Parameter	Value	Unit	Note
Module Form Factor	QSFP+		
Number of Lanes	4 Tx and 4 Rx		
Maximum Aggregate Data Rate	42.0	Gb/s	
Maximum Data Rate per Lane	10.5	Gb/s	
Protocols Supported	Typical applications include 40G Ethernet, Infiniband, Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	38-pin edge connector ,Pin-out as defined by the QSFP+ MSA		
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		

Parameter	Symbol	Min	Typ	Max	Units	Note
Bit Rate per Lane	B_R	1062		10500	Mb/sec	1
Bit Error Ratio	B_{ER}			10-12		2
Distance on OM3 MMF (D1)	D_1			100	meters	3
Distance on OM4 MMF (D2)	D_2			150	meters	3
Distance on OM3 MMF (D3)	D_3			300	meters	4
Distance on OM4 MMF (D4)	D_4			400	meters	4

Notes:

1. Compliant with 40G Ethernet. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fiber Channel.
2. Tested with a PRBS 2^{31-1} test pattern.
3. 40GBASE-SR4, IEEE 802.3ba

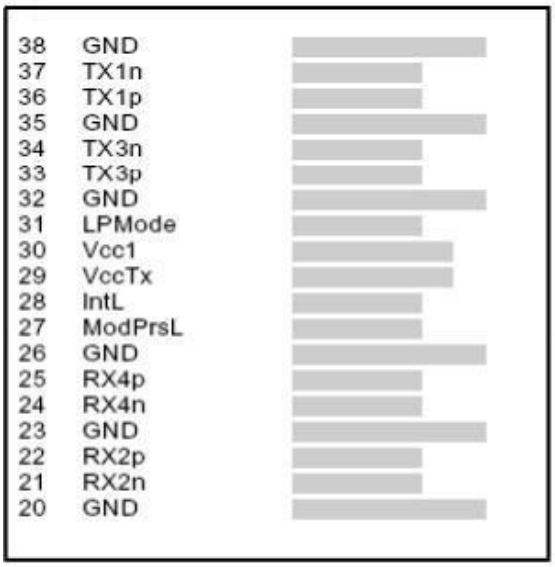
Optical Characteristics ($T_{OP(C)}$ = 0 to 70 ℃, $T_{OP(I)}$ =-40 to 80 ℃, V_{CC} = 3.13 to 3.47 V)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Transmitter						
Operating Wavelength	λ	840	850	860	nm	
Ave. output power (Enabled)	P_{AVE}	-7.5		+2.5	dBm	
Difference in launch power between any two lanes (OMA)	D_L			4	dB	
Extinction Ratio	E_R	3			dB	
Peak power, each lane	P_P			4	dBm	
Dispersion penalty, each lane	T_{DP}			3.5	dB	
Average launch power of OFF transmitter, each lane	P_{OFF}			-30	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio = 5x10-5
Receiver						
Operating Wavelength	λc	840	850	860	nm	
Stressed receiver sensitivity in OMA	P_{SEN1}			-5.4	dBm	3
Stressed receiver sensitivity in OMA	P_{SEN2}			-7.5	dBm	3
Average Receive Power, each lane	P_{AVE}	-11		+2.4	dBm	
Receiver Reflectance	Rrx			-12	dB	
LOS Assert	Pa	-30			dBm	
LOS De-assert	Pd			-9	dBm	
LOS Hysteresis	Pd-Pa	0.5			dB	

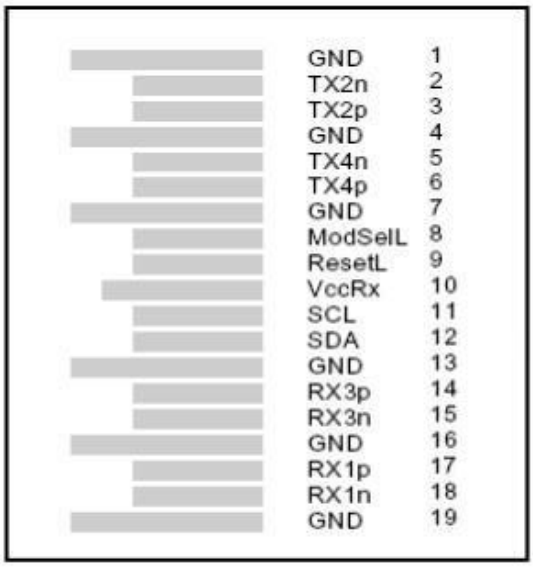
Notes:

1. Measured with conformance test signal at TP3 for BER = 10^{-12} Receiver Characteristics

Pin defintion and Functions



Top side



Bottom side

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	1
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	Non-Inverted
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1

27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.

Other Pin Description:

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

QSFP+ SR4 operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

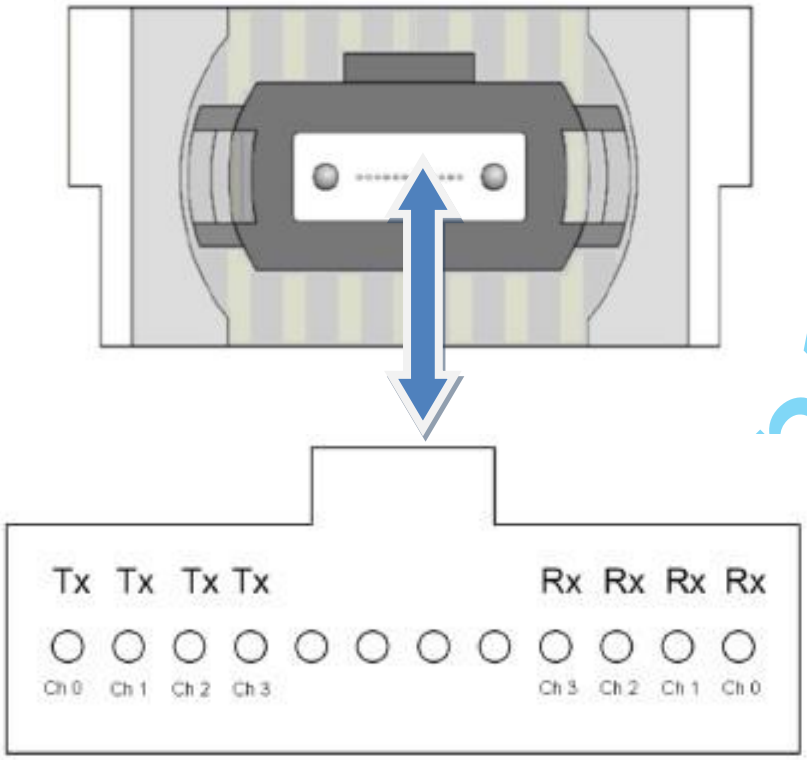
ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

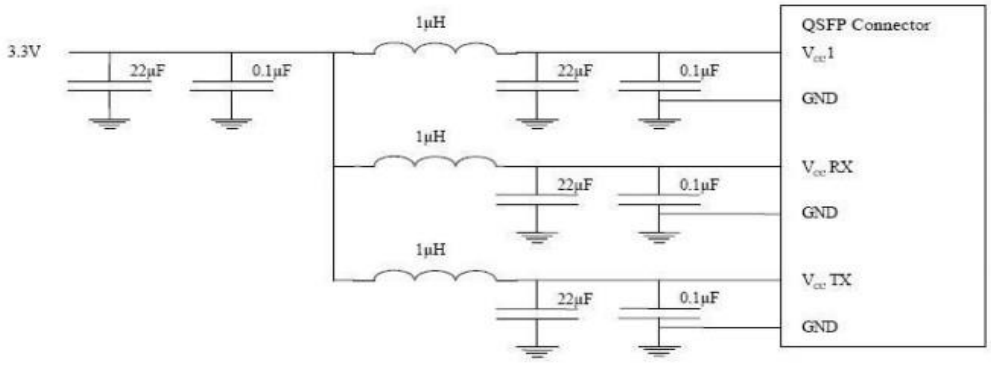
IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

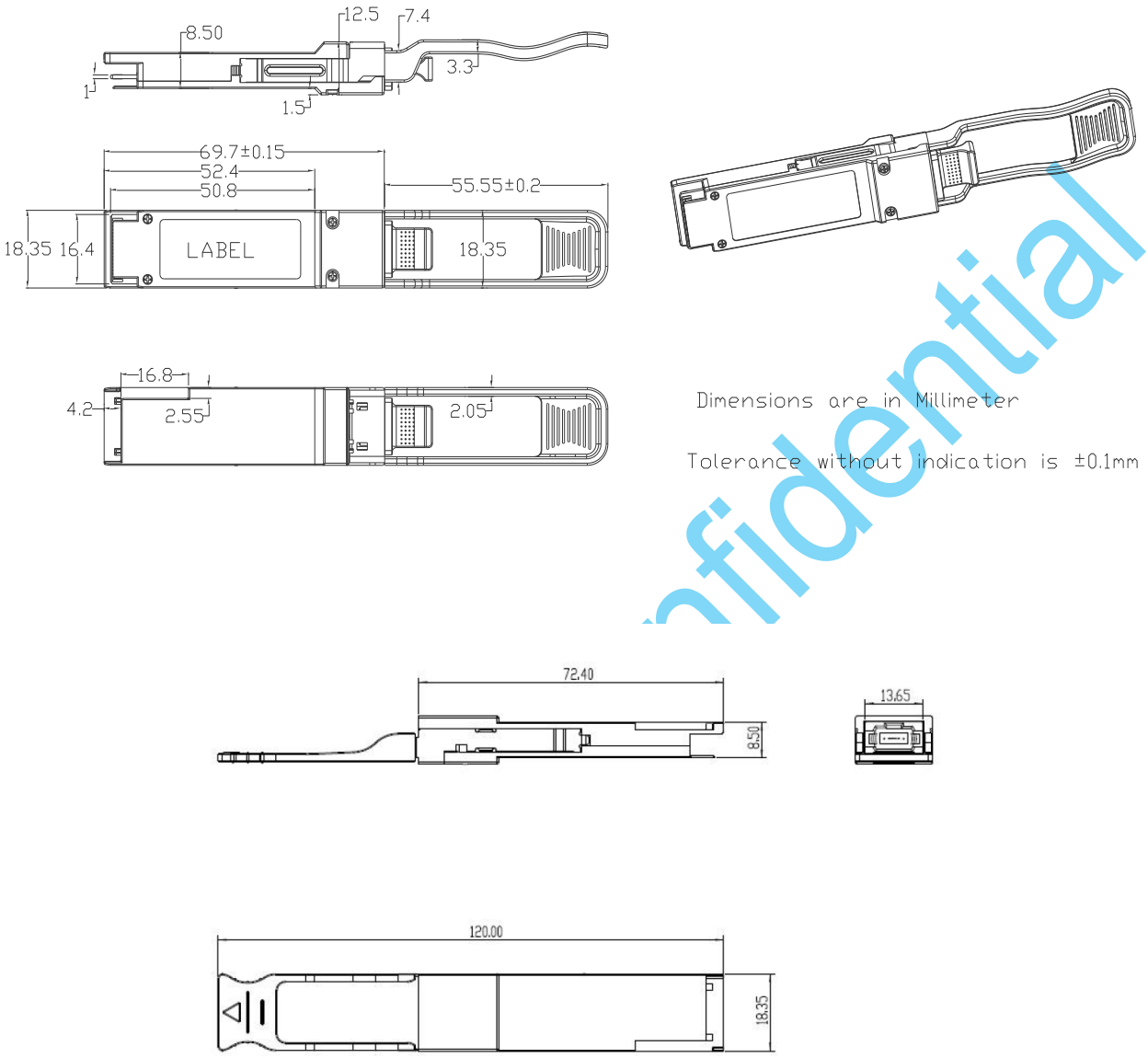
Optical lane assignment (front view of MPO receptacle)



Power Supply Filtering



Package Dimensions



Order information

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