

Applications

- InfiniBand QDR, DDR and SDR
- 40G Ethernet
- Proprietary High Speed Interconnections
- Data center

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.3	3.6	V	
Storage Temperature	Ts	-40	85	°C	
Relative Humidity	RH	0	85	%	
Damage Threshold, per Lane	DT	3.4		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

General Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Note
Bit Rate per Lane	BR			10.313	Gb/s	1
Bit Error Ratio	BER			10 ⁻¹²		2
Distance on SMF	D1			10	Km	3

Notes:

1. Compliant with 40G Ethernet. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fiber Channel.
2. Tested with a PRBS 2³¹⁻¹ test pattern.
3. Per 40GBASE-LR4, IEEE 802.3ba.

Optical Characteristics (T_{OP(C)} = 0 to 70 °C, V_{CC} = 3.13 to 3.47 V)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Transmitter						
Operating Wavelength	λc	1270	1310	1350	nm	
Ave. output power	P _{AVE}	-5.2		+1	dBm	
Difference in launch power between any two lanes (OMA)	D _L			5	dB	
Extinction Ratio	E _R	3.5			dB	
Peak power, each lane	P _P			4	dBm	
Dispersion penalty, each lane	T _{DP}			3.5	dB	
Average launch power of OFF	P _{OFF}			-30	dB	

transmitter, each lane						
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio = 5x10-5
Receiver						
Operating Wavelength	λ_c	1270		1350	nm	
Stressed receiver sensitivity in OMA(TNQS314XL-CD104)	P _{SEN1}			-12.5	dBm	3
Average Receive Power,each lane	P _{AVE}	-11		+2.4	dBm	
Receiver Reflectance	R _{Rx}			-12	dB	
LOS Assert	P _a	-30			dBm	
LOS De-assert	P _d			-15	dBm	
LOS Hysteresis	P _d -P _a	0.5			dB	

Notes:

1. Measured with conformance test signal at TP3 for BER = 10⁻¹² Receiver Characteristics

Pin Defintion And Functions

38	GND	
37	TX1n	
36	TX1p	
35	GND	
34	TX3n	
33	TX3p	
32	GND	
31	LPMode	
30	Vcc1	
29	VccTx	
28	IntL	
27	ModPrsL	
26	GND	
25	RX4p	
24	RX4n	
23	GND	
22	RX2p	
21	RX2n	
20	GND	

Top side

	GND	1
	TX2n	2
	TX2p	3
	GND	4
	TX4n	5
	TX4p	6
	GND	7
	ModSelL	8
	ResetL	9
	VccRx	10
	SCL	11
	SDA	12
	GND	13
	RX3p	14
	RX3n	15
	GND	16
	RX1p	17
	RX1n	18
	GND	19

Bottom side

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	1

9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver	Non-Inverted
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power S	
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.

Other Pin Descriptions:

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMODE_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to their default state.

Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMoDe Pin

QSFP+ PSM LR4 operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

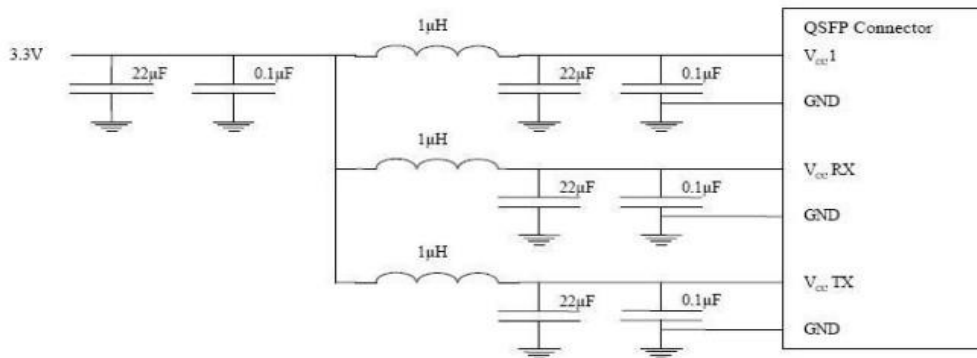
ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

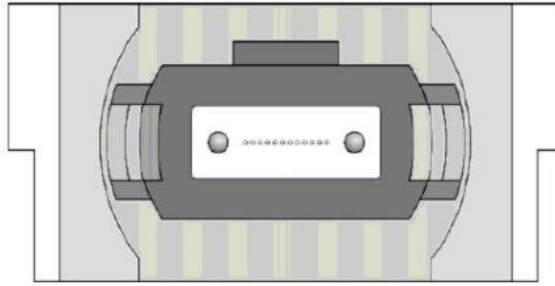
IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

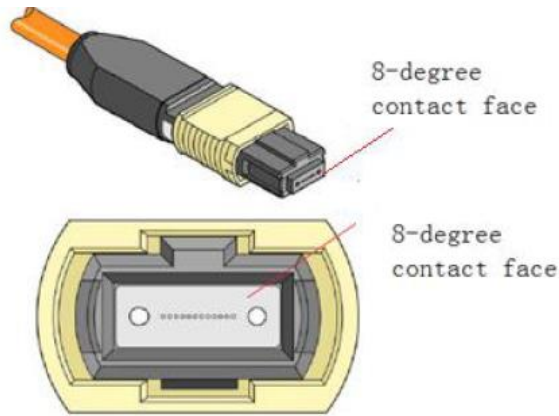


Optical Interface Lanes and Assignment

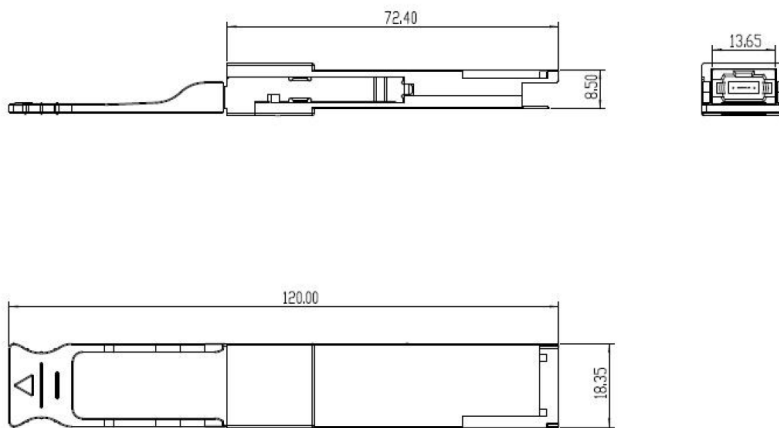
The optical interface port is a male MPO connector. The four fiber positions on the left as shown in below, with the key up, are used for the optical transmit signals (Channel1 through4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.



Transmit Channels: 1 2 3 4
 Unused positions: x x x x
 Receive Channels: 4 3 2 1



Package Dimensions



Order information

Part Number	Description
TNQS314XL-CD104	QSFP+ 40G LR4 Optical Transceiver